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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,445	07/18/2003	Yasuo Yamagishi	030868	1112

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,445	YAMAGISHI ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *3,5,8,9 and 12-31* is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 11* is/are allowed.

6)☒ Claim(s) *1-2,4 and 6-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claim 1-2, 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horel et al (4862077).

Regarding claim 1, Horel et al disclose [see Fig. 2A] a probe card (probe card 30) for testing a semiconductor chip [not shown but see col. 1, lines 16-24], comprising: plurality of probes (spring load contact pins 61-63); build-up interconnection layer (probe card member 31) having a multilayer interconnection structure (first board 31a and second board 31b) therein, said build-up interconnection layer (31) carrying said plurality of probes (61-63) on a top surface thereof in electrical connection with said multilayer interconnection structure (31a and 31b); and a capacitor (electronic component E4) embedded resin insulation layer (adapter ring 33)

constituting said build-up interconnection layer (31) in electrical connection with one of said probes (61-63) via said multilayer interconnection structure (31a and 31b), said multilayer interconnection structure (31a and 31b) including an inner via-contact (contact holes 51-54) in the vicinity of said probe (61-63). However, they do not disclose the capacitor entirely within a resin insulation layer. It is well known to make capacitor entirely within a resin insulation layer where needed (see MPEP 2144.04; *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950)). It would have been obvious to one or ordinary skill in the art at the time of the invention to make the capacitor entirely within a resin insulation layer since the rearrangement of the capacitor would be matter of design choice to each individual user and also it would not have modified the operation of the device.

Regarding claim 2, Horel et al disclose said capacitor (E4) has a thickness generally equal to or less than a thickness of said resin insulation layer (33) [see Fig. 2A].

Regarding claim 4, Horel et al disclose said capacitor (E4) is formed in said build-up interconnection layer (31) [via adapter ring 33]. However, they do not disclose the capacitor is right underneath one of said probes. It is well known to make capacitor right underneath one of the probes where needed (see MPEP 2144.04; *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950)). It would have been obvious to one or ordinary skill in the art at the time of the invention to make the capacitor to be right underneath one of the probes since the rearrangement of the capacitor would be matter of design choice to each individual user and also it would not have modified the operation of the device.

4. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horel et al (4862077) in view of Fukuzumi et al (6548844).

Regarding claim 6, Horel et al disclose [see Fig. 2A] a probe card (probe card 30) for testing a semiconductor chip [not shown but see col. 1, lines 16-24], comprising: a capacitor (electronic component E4) embedded resin insulation layer (adapter ring 33) constituting said build-up interconnection layer (31) in electrical connection with one of said probes (61-63) via said multilayer interconnection structure (31a and 31b). However, they do not disclose the feature of the capacitor as claimed. Fukuzumi et al disclose [Fig. 1] a capacitor structure 1 includes a dielectric film (capacitor dielectric film 3) of a complex oxide containing at least one metal element selected from the group consisting of Sr, Ba, Pb, Zr, Mg and Nb [see col. 5, lines 25-38]. Further, Fukuzumi et al teach that the addition of features of the capacitor is advantageous because it suppresses the deterioration of the data retaining characteristic that is originated from when annealing is performed in an atmosphere containing a reduce agent. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Horel et al by adding the features of the capacitor as taught by Fukuzumi et al in order to suppress the deterioration of the data retaining characteristic that is originated from when annealing is performed in an atmosphere containing a reduce agent.

Regarding claim 7, Horel et al disclose [see Fig. 2A] a probe card (probe card 30) for testing a semiconductor chip [not shown but see col. 1, lines 16-24], comprising: a capacitor (electronic component E4) embedded resin insulation layer (adapter ring 33) constituting said build-up interconnection layer (31) in electrical connection with one of said probes (61-63) via said multilayer interconnection structure (31a and 31b). However, they do not disclose the feature of the capacitor as claimed. Fukuzumi et al disclose [Fig. 1] a capacitor structure 1 includes an upper (common electrode 4) and lower (dispersion electrode 2) electrodes

sandwiching a dielectric film (capacitor dielectric film 3), said upper (4) and lower (2) electrodes containing at least one metal element or a metal oxide selected from the group consisting of Pt, Au, Cu, Pb, Ru, a Ru oxide, Ir, an Ir oxide, and Cr [see col. 5, lines 43-45 and col. 6, lines 8-25]. Further, Fukuzumi et al teach that the addition of features of the capacitor is advantageous because it suppresses the deterioration of the data retaining characteristic that is originated from when annealing is performed in an atmosphere containing a reduce agent. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Horel et al by adding the features of the capacitor as taught by Fukuzumi et al in order to suppress the deterioration of the data retaining characteristic that is originated from when annealing is performed in an atmosphere containing a reduce agent.

Election/Restrictions

5. This application contains claims 12-31 drawn to an invention nonelected without traverse in Paper No. 12/1/04. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kohler et al (3932810), and Mori et al (6818469) disclose different features of a capacitor for a semiconductor device.

7. Applicant's arguments filed March 10, 2005 have been fully considered but they are not persuasive.

Applicant's argues: "Applicants respectfully disagree "E4" represents an electronic component, which is not necessarily a capacitor, which "can be soldered on the top surface of the adapter ring 33 between the contact hole 53' and the central pound region 46", as disclosed in column 11, lines 3-6. This is in contrast to the present invention, in which the capacitor 20 is embedded entirely within resin insulation layer 14, as shown in Fig. 4."

In response to the above arguments, Horel et al disclose that electronic component "E4" is a capacitor. In col. 11, lines 35-36 it states: "... a parallel circuit from the T-shaped circuit to ground has been introduced by the 0.1 microfarad capacitor E4..." Further, the capacitor is embedded entirely in the resin layer is a matter of design choice to each individual user.

8. Claims 10-11 are allowed over the prior art.

9. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 10, the primary reason for the allowance of the claim is due to the specific limitation of a test method of a semiconductor device comprising the step of before contacting said probe card to said semiconductor chip, of setting an impedance between said probe and said capacitor to be substantially equal to an impedance of a semiconductor package including therein said semiconductor chip and a capacitor, for a part between said semiconductor chip and said capacitor. Since claim 11 depends from claim 10, it is also have allowable subject matter.

Since the examiner is maintaining the same rejection, the following is given.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
June 22, 2005